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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/598,514	01/29/2007	Chuen Khiang Wang	P26634	6698

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EXAMINER	
AHMED, SELIM U	
ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
11/02/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/598,514	WANG ET AL.	
	Examiner	Art Unit	
	SELIM AHMED	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *2-4,14,23,24 and 26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-13,15-22,25 and 27-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/21/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's remark filed on 06/16/2009 is acknowledged. Applicant noted that the HABA et al. publication (U.S. Pub. No. 2005/0285246) has an effective filing date in the United States of June 25, 2004. Since the present application has an effective filing date in the United States of March 3, 2004, the present application has an effective filing date before the effective filing date of the HABA et al. publication. Thus, the rejection cannot be properly based on 35 U.S.C. § 102. Furthermore, applicants noted that KHIANG et al. (U.S. Pub. No. 2003/0197284) does not qualify as prior art against the present application for purposes of a rejection under 35 U.S.C. § 103 (a) due to common ownership with the present application.

So, non-final rejection sent on 03/17/2009 has been vacated accordingly. Also, previously indicated allowability of claims 8-10 have been withdrawn as these claims have been rejected with newly discovered references under this office action..

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 11-13, 15-22, 29, 30, 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li (US 2004/0108581) in view of Isaak et al (US 2001/0035572, Isaak hereinafter).

With regard to claim 1, Li discloses a semiconductor package e.g. Figs. 1-9 comprising: a first substrate 10 having a die receiving area (area where die is attached), a first adhesive layer 35, a window opening 211 and a plurality of conductive traces (22a, 22b, 22c); a first semiconductor die 24, having an electrically active side (26) and an electrically inactive side (28), the electrically active side 26 being mounted to said first substrate 10 through the first adhesive 35 at the die receiving area, to electrically couple said first semiconductor die 24 to the plurality of conductive traces 22a, 22b, 22c (according to para[0041], pads (22a, 22b, 22c) of substrate 10 are connected to contact 27, conductive member i.e. 2nd substrate 40 and the 2nd contact 50) ; a second adhesive layer 37 having a first side attached to an electrically inactive side (28) of said first semiconductor die 24; a second substrate 40 having a die receiving area (area where 45 attached), and a side 56 with terminals (where bond wire contacts); a third adhesive layer 42 having a first side (side that faces 40) attached to the side of said second substrate 40 with the terminals (e.g. Fig. 7); a last semiconductor die 45, having an electrically active side 48 and an electrically inactive side 52, the electrically inactive side 52 being mounted to the second side of said third adhesive layer 42, and the electrically active side 48 being electrically coupled to

said conductive traces 22a, 22b, 22c (para [0041]) of said first 10 or second substrate 40 directly or through a redistribution device; an encapsulant (abstract) to encapsulate said semiconductor dies and electrical coupling (Fig. 7); and signal interconnections 60a, 60b, 60c to transfer an electrical signal from said conductive traces 22a, 22b, 22c to an exterior of the package (Fig. 7).

As discussed above, Li's Figs. 1-7 discloses all of the limitations of claim 1 with the exception of the first substrate having a window opening. However, in Fig. 9 (different embodiment), Li discloses a substrate 210 having a window opening 211. As it is known in the art, electrical connection can be made between the chip and outer pad of the substrate through the window opening by electrical wire. Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to include a substrate with window opening as shown by Li for predictable results.

Furthermore, Li's Figs. 1-7 discloses all of the limitations of claim 1 but does not explicitly disclose the second substrate 40 having a plurality of conductive traces although a side with terminals (terminals that connect 22c through wire) is evident in Fig.7. Para[0043] of Li discloses, "The substrate 10 may comprise one or more layers and may incorporate other features, such as traces or conductive planes. The pads and terminals carried by the substrate desirably comprise conductive materials commonly used to form electrical

connections and used in making microelectronic elements and microelectronic components, such as copper and gold". Since Li discloses substrate 10 having traces or conductive plane, it would have been obvious to one having ordinary skill in the art at the time of the invention to have conductive traces on the second substrate 40 for electrical connection. Furthermore, fig. 5, para [0040] of Issak disclose a substrate 26 having a plurality of conductive traces 40 a side with terminals 38. It would have been obvious to one having ordinary skill in the art at the time of the invention to substitute Li's substrate with Isaak's substrate having a plurality of conductive traces with a side with terminals for transmitting electrical signal within the conductive traces and external interconnection.

With regard to claim 11, e.g. Fig. 7 of Li discloses the semiconductor package according to claim 1, wherein the size of said first semiconductor die 24 may be smaller, equal to, or greater than the size of said last semiconductor die 45.

With regard to claim 12, e.g. Fig. 9 of Li discloses the semiconductor package according to claim 1, wherein the electrical coupling from said first semiconductor die to said first substrate is by wire bond 258.

With regard to claim 13, it does not distinguish over the Li reference regardless of the process used to electrical coupling from said first semiconductor die to said first substrate because only the final product is

relevant, not the process of making such as "TAB method". Note that a "product by process claim" is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in " product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

With regard to claim 15, e.g. Fig.7 of Li discloses the semiconductor package according to claim 1, wherein the first semiconductor die 25 is electrically coupled to the first substrate 10 by a flip chip method.

With regard to claim 16, Li in view of Issak discloses all of the limitations of claim 1 with the exception of wherein said last semiconductor die is electrically coupled to said second substrate by a flip chip method. However, according to Fig. 2 of Li, a first IC device is coupled to the substrate by a flip-chip method, which is well known in the art. So, similar to claim 15 rejection and Fig.2 of Li, it would have been obvious to one having ordinary skill in the art at the time of the invention to electrically couple the last semiconductor die to said second substrate by a flip chip method.

With regard to claim 17, in light of claim 16 rejection above, e.g. Fig. 7 of Li discloses the semiconductor package according to claim 1, wherein said last semiconductor die is stacked with an inactive side facing an inactive side of a flip chip semiconductor die on said second substrate.

With regard to claim 18, e.g. para[0039] of Li discloses the semiconductor package according to claim 1, wherein said second substrate is formed of any of the following materials including silicon, ceramic, laminate, aluminum, and any material that can be manufactured with a plurality of conductor traces.

With regard to claim 19, e.g. Fig. 5 of Li discloses the semiconductor package according to claim 1, wherein said second substrate 40 is formed of a

thin laminate, a flexible circuit, or a lead- frame and processed to increase rigidity for attachment and an electrical interconnection process.

With regard to claim 20, e.g. Fig. 7 of Li discloses the semiconductor package according to claim 1, wherein said second substrate 40 has terminals (where 58 connects) along its periphery allowing interconnects to convey electrical signals to and from said last semiconductor die 45 and said first substrate at any side of said last semiconductor die 45 (since chip 45 is connected to 22b and 40 is connected 22c; and 22b & 22c are connected, electrical signal can be conveyed between 40 and 45).

With regard to claims 21 and 22, Li (in view of Isaak) discloses all of the limitations of claim 1 and Fig. 7 of Li further discloses said second substrate 40 having the terminals (that connect to 22c) positioned in optimum positions along its periphery (Fig. 7) such that wire bonding from the terminals to said first substrate allow shortest interconnection paths to the package external pins or from said first semiconductor die to the terminals (Fig. 7). Additionally, e.g. Figs. 2, 4, 5, para [0040] of Isaak further disclose a substrate 26 includes a plurality of conductive traces 40 having the terminals 38. It would have been obvious to one having ordinary skill in the art at the time of the invention to combine feature of Li's substrate with Isaak's substrate and results would have been predictable.

With regard to claim 29, e.g. abstract of Li discloses the semiconductor package according to claim 1, wherein said encapsulant is applied to the package to cure.

With regard to claim 30, e.g. Fig. 7, abstract of LI discloses the semiconductor package according to claim 1, wherein said encapsulant comprises a lid to cover said semiconductor die and electrical coupling.

With regard to claim 31, Li in view of Isaak discloses the semiconductor package according to claim 1, wherein all the adhesive layers can be pre-attached to a receiving area or to a matching side of a part to attach to the receiving area (Functional limitations "can be" not given significant patentable weight since all the adhesive layers can be pre-attached to a receiving area or to a matching side of a part to attach to the receiving area).

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li in view of Isaak and further in view of Tao et al (US 6,118,176; Tao hereinafter).

With regard to claim 5, Li in view of Isaak discloses all of the limitations of claim 1 including said last semiconductor die 45 has a plurality of bond pads 50 (fig. 7), but with the exception of whereby said bond pads are not positioned near the periphery of said last semiconductor die, said bond pads being electrically

relocated to the periphery of said last semiconductor die by a redistribution device. However, e.g. in Fig. 4 of Tao discloses said bond pads 407 are not positioned near the periphery of said last semiconductor die 401, said bond pads 407 being electrically relocated to the periphery of said last semiconductor die 401 by a redistribution device 406. It would have been obvious to one having ordinary skill in the art at the time of the invention to include redistribution devices of Tao within Li and Isaak's device and results would have been predictable i.e. reducing the risk of interference of the electrical connections.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li in view of Isaak in view of Tao and further in view of Yang et al (US 2004/0124539; Yang hereinafter).

With regard to claim 6, Li in view of Isaak further in view of Tao discloses all of the limitations of claim 5 as discussed above, furthermore Fig. 2, para[0004, 0005] of Yang discloses said redistribution device includes a wafer i.e. dummy chip redistribution layer 130. It would have been obvious to one having ordinary skill in the art at the time of the invention to include a wafer redistribution layer within Li's device and results would have been predictable i.e. electrical connection interface.

5. Claims 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li in view of Isaak in view of Tao or Yang as applied to claim 5 or 6 respectively and further in view of Foster et al (US 6,603,072; Foster hereinafter).

With regard to claim 7 and 8, Li (in view of Isaak, Tao or Yang) discloses all of the limitations of claim 5 or 6 respectively with the exception of said redistribution device includes a metallic interposer with a plurality of conductive traces, attached to the active surface of the last semiconductor die with an adhesive, with a plurality of electrical couplings from the bond pads to the metallic interposer. However, Figs. 7, 8 of Foster disclose said redistribution device 780 includes a metallic interposer 80 with a plurality of conductive traces 86. Furthermore, Fig. 4 of Tao discloses a plurality of conductive traces (col.4, lines 1-40) attached to the active surface of the last semiconductor die 401 with an adhesive (col.4, lines 1-40), with a plurality of electrical couplings 408 from the bond pads to the metallic interposer. It would have been obvious to one having ordinary skill in the art at the time of the invention to include metallic interposer as Foster discloses and attached to the active surface of the last semiconductor die with an adhesive, with a plurality of electrical couplings from the bond pads to the metallic interposer and include within Li's device and results would have been predictable i.e. reducing the risk of interference of the electrical connections.

With regard to claim 9 and 10, e.g. col.4, lines 1-40 of Tao discloses the semiconductor package according to claim 8, wherein said adhesive is an adhesive paste or coating or an adhesive film.

6. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li in view of Isaak and further in view of Her et al (US 2002/0180023; Her hereinafter).

With regard to claim 25, Li in view of Issak discloses all of the limitations of claim 1 with the exception of the semiconductor device further comprising a spacer in the stacking of the semiconductor dies. However, in Fig. 4B of Her discloses the semiconductor device further comprising a spacer 420a in the stacking of the semiconductor dies. It would have been obvious to one having ordinary skill in the art at the time of the invention to include a spacer in between dies to form stacked dies to separate the dies from each other.

7. Claims 27, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li in view of Isaak and further in view of Bolken et al (US 2004/0178482; Bolken hereinafter).

With regard to claim 27, or 28, Li in view of Isaak discloses all of the limitations of claim 1 with the exception of the semiconductor package wherein said encapsulant is a liquid encapsulant or wherein said encapsulant is a transfer

molded molding compound respectively. However, e.g. claim 5, 7 of Bolken discloses all of the above specified limitations. It would have been obvious to one having ordinary skill in the art at the time of the invention to encapsulate the device of Li as disclosed by Bolken for protecting the device from outside environment.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SELIM AHMED whose telephone number is (571)270-5025. The examiner can normally be reached on 9:00 AM-6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571)272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SA/

/Ben P Sandvik/
Examiner, Art Unit 2826